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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,653	06/25/2003	Berthold Wedding	Q76008	1047
SUGHRUE MI	-	EXAMINER SINKANTARAKORN, PAWARIS		
2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			ART UNIT	PAPER NUMBER
WASHINGTO	WASHINGTON, DC 20037		2616	-
SHORTENED STATUTOR	Y PERIOD OF RESPONSE	MAIL DATE	DELIVER	Y MODE
3 MONTHS		03/09/2007	· PAPER	

# Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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	Application No.	Applicant(s)					
	10/602,653	WEDDING, BERTHOLD					
Office Action Summary	Examiner	Art Unit					
	Pao Sinkantarakorn	2616					
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to communication(s) filed on 25 Ju	ne 2003.						
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•							
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4) Claim(s) <u>1-9</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-9</u> is/are rejected.							
7) Claim(s) is/are objected to.	7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	election requirement.						
Application Papers							
9)⊠ The specification is objected to by the Examine	r.						
10)⊠ The drawing(s) filed on <u>25 June 2003</u> is/are: a)  accepted or b)⊠ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)⊠ All b)□ Some * c)□ None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
3. Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	ate					
<ol> <li>Information Disclosure Statement(s) (PTO/SB/08)</li> <li>Paper No(s)/Mail Date <u>10/10/2003</u>.</li> </ol>	5)  Notice of Informal P 6)  Other:	arent uphinarion					

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#### **DETAILED ACTION**

#### **Drawings**

- The drawings are objected to because there is no descriptive legend in figure 4. 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- 2. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37

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CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

#### Specification

3. The disclosure is objected to because, **regarding paragraph 37 line 3**, the term "figure 1" should be changed to "figure 4" because the switching element has only been mentioned in figure 4.

Appropriate correction is required.

#### Claim Objections

4. Claim 7 is objected to because, on line 3, the term "a said data signal" should be changed to "said data signal".

Appropriate correction is required.

## Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. (US 5,457,718).

Anderson et al. disclose, **regarding claim 1,** an input circuit for phase controlling of a data input signal with a clock signal, comprising:

a flip-flop (see figure 1 reference numeral 30), wherein the data signal is fed to a clock input of the flip-flop (see figure 1, line RD into the clock input of reference numeral

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30) and the clock signal is fed to the data input of the flip-flop (see figure 1, line CLK into the data input of reference numeral 30), and wherein the data output of the flip-flop is used as a control signal of a locked loop (see figure 1, PTLEAD and column 3 lines 59-63);

regarding claim 2, a further flip-flop (see figure 1 reference numeral 50), wherein the data signal is fed to a data input of the further flip-flop (see figure 1, line RD into the data input of reference numeral 50) and the clock signal is fed to the clock input of the further flip-flop (see figure 1, line CLK into the clock input of reference numeral 50);

regarding claim 3, the data input signal being provided by output data of a data source (see figure 1, reference numeral 20), wherein the data source is arranged to control the phase of the output data in dependence of an adjusting signal which is input to the data source (see column 3 lines 61-63, the output of the digital filter 40 controls the phase of the amount of delay of data element 20), wherein the locked loop delivers the adjusting signal to the data source (see figure 1, reference numeral 4 from the output of the digital filter 40).

### Claim Rejections - 35 USC § 103

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

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not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

- 8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  - 1. Determining the scope and contents of the prior art.
  - 2. Ascertaining the differences between the prior art and the claims at issue.
  - 3. Resolving the level of ordinary skill in the pertinent art.
  - 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
- 9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**NOTE**: In claim 6 line 2, the recitation "thus being a delay locked loop" is not considered a claimed limitation because it is in parentheses; therefore, it is suggested applicant to remove it.

10. Claims 4-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. in view of Farjad-Rad et al. (US 5,799,048).

Anderson et al. disclose, **regarding claim 4-6**, an input circuit applied to claim 2 above, wherein the locked loop comprises a controllable phase shifter (see figure 1 reference numeral 20, and column 3 lines 61-63, the output of the digital filter is dependent of the variable delay 20, which means the digital filer is controllable through

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the variable delay 20) and is arranged to adjust the phase of the data input signal, which is provided to the clock input of the further flip-flop and the data input of the flip-flop (see column 3 lines 61-64).

Anderson et al. also disclose, **regarding claim 9**, a method for phase controlling of a clock signal with a data signal comprising:

scanning the clock signal with an edge of the data signal (see column 3 lines 58-60);

deriving from the scanning result a control signal (see column 3 lines 59-64); and using the control signal for adjusting the phase relationship between the data signal and the clock signal (see column 3 lines 61-62).

Anderson et al. do not disclose an input circuit wherein the locked loop is arranged to adjust the phase of the clock signal, as recited in claim 4-6, nor phase controlling of a data signal with a clock signal. The invention of Farjad-Rad et al. from the same or similar fields of endeavor disclose an apparatus, which is arranged to adjust the phase of the clock signal (see column 4 lines 65-67).

Thus, it would have been obvious to the person of ordinary skill in the art to implement/modify a method of adjusting the phase of the clock signal into the locked loop circuit of Anderson et al by adding a voltage-controlled oscillator (VCO) in the circuit and instruct the VCO to adjust the phase of the clock signal (see column 4 lines 65-67).

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The motivation for implementing a method of adjusting the phase of the clock signal is that it provides a more efficient data transmission because the clock and data signals can be synchronized to avoid loss of data (see column 1 lines 12-20).

#### Claim Rejections - 35 USC § 103

- 11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 12. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. in view of Watson, Jr. et al. (US 5,272,390).

Anderson et al. disclose, **regarding claims 7 and 8**, an input circuit applied to claim 1 and 2 above, wherein the data signal is fed to a clock input of the flip-flop (see figure 1, line RD into the clock input of reference numeral 30).

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flops, which correspond to the number of the of data inputs of the multiplexer, reference numeral 118 is the clock signal being fed to the clock input of the multiplexer).

Thus, it would have been obvious to the person of ordinary skill in the art to implement/modify a multiplexer having a plurality of data inputs, wherein the clock signal is fed to the clock input of the multiplexer and a number of further flip-flops for a plurality of data signals is provided, which number corresponds to the number of data inputs of the multiplexer into the locked loop circuit by Anderson et al. by connecting the output of the further flip-flops to the plurality of data inputs of the multiplexer and connecting the clock signal to the clock input of the multiplexer.

The motivation for implanting a multiplexer having a plurality of data inputs, wherein the clock signal is fed to the clock input of the multiplexer and a number of further flip-flops for a plurality of data signals is provided, which number corresponds to the number of data inputs of the multiplexer being that it provides better synchronization of the circuit because flip-flops synchronizes multiplexer data.

#### Conclusion

- 13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kizer et al. (US 6,759,881) and Donnelly et al. (US 6,125,157) are cited to show apparatuses that are considered pertinent to the claimed invention.
- 14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pao Sinkantarakorn whose telephone number is 571-270-1424. The examiner can normally be reached on Monday-Thursday 7:30am-4:00pm EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang B. Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KWANG BIN YAO PRIMARY EXAMINER

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